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ABSTRACT OF THE DISCLOSURE

The present invention integrates a phase lock loop (PLL) with a programmable logic device (PLD) to realize a flexible PLD with a variety of clocking options. The present invention generates multiple clock frequencies internally to a programmable logic device using a single reference clock input. The programmer can dynamically change the functionality of the programmable logic device. As a result, a "virtual hardware device" is realized. The ability to change the frequency of operation also dynamically offers a tremendous advantage to users of reconfigurable computing.